REMARKS

The Examiner's Action mailed on March 30, 2005, has been received and its contents carefully considered. Additionally attached to this Amendment is a Petition for Three-month Extension of Time, extending the period for response to expire on September 30, 2005. Also attached is payment for the fee of $200.00 for 4 further claims in excess of 20.

In this Amendment, Applicant has amended claims 1, 2 and 20, and added new claims 28 through 31. Claims 1 and 28 are the independent claims, and claims 1-31 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has objected to the Abstract for an informality. Attached hereto is a corrected Abstract, which complies with all official provisions.

The Examiner's Action has rejected claims 1-22 under 35 U.S.C.103(a) as being unpatentable over Norman et al. in view of Asada et al. It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Claim 1 recites, *inter alia*, a combined semiconductor apparatus, that includes first and second semiconductor films, which are both disposed on and bonded to the same surface side of a substrate.

One effect of the invention of claim 1 is that since the first and second thin semiconductor films are thin and small, costs of the first and second thin semiconductor films can be reduced. Another effect of the invention of claim 1 is

that since the first thin semiconductor film and the second thin semiconductor film are electrically connected by a first individual interconnecting line formed as a thin film, no wire-bonding pad areas for electrically connecting the thin semiconductor films are needed, thereby reducing a substrate upside surface area and assembly costs. In addition, since no wire-bonding is needed, the rate of occurrence of interconnection faults is reduced and the combined semiconductor apparatus with high reliability can be obtained.

The Examiner's Action states that Norman et al. disclose a method of fabricating an integrated multicolor or single color organic LED array, which comprises a substrate (12), and a first thin semiconductor film (electron transport layer 14 and organic layer 15) (col. 3, lines 5-16) disposed on and bonded to the substrate. The first thin semiconductor film includes at least one semiconductor device (each of the organic layers 15, 20, 25 corresponds to a particular color LED device). A second thin semiconductor film is allegedly disposed on and bonded to the substrate, with the second thin semiconductor film including an integrated circuit (integrated circuit driver using thin film transistor (FET) 50).

The Examiner's Action states that the second thin semiconductor film in Norman et al. includes an integrated circuit, i.e., in an integrated circuit driver using thin film transistor (driver IC) 50. However, it is respectfully submitted that Norman et al. fail to disclose or suggest a second thin semiconductor film as recited in claim 1 of the present application.

In particular, the FET 50 disclosed by Norman et al. is formed inside the substrate 12, which is a semiconductor substrate made of silicon or gallium arsenide. Therefore, as is obvious from Figures 6 and 9 of Norman et al., the FET 50 is a feature of the substrate 12. Moreover, the substrate 12 of Norman et al. is a typical semiconductor substrate for a semiconductor device and therefore is thick and rigid.

On the other hand, the Examiner's Action indicates that the substrate of claim 1 of the present application corresponds to the substrate 12 of Norman et al., as shown in line 4, item 5 of the Office Action. Thus, in the Examiner's opinion, the substrate 12 of Norman et al. corresponds to both the substrate of claim 1 and the second thin semiconductor film of claim 1.

In contrast, the second thin semiconductor film of claim 1 of the present application, is disposed on and bonded to same surface side of the substrate as the first thin semiconductor film. This feature is not disclosed or suggested by Norman et al.

That is, and stated alternatively, assuming that that the substrate 12 of Norman et al. corresponds to the substrate of claim 1 of the present application, it necessarily follows that there is no second thin semiconductor film disposed on and bonded to a surface thereof, in the Norman et al. patent.

Alternatively, assuming that the substrate 12 of Norman et al. corresponds to the second thin semiconductor film of claim 1 of the present application, it

necessarily follows that there is no substrate having a second thin semiconductor film disposed on and bonded to a surface thereof.

Further, the substrate 12 of Norman et al. supports layers 13, 14, 15, 20 and 25, and is made of a rigid and fat material, and therefore it is not a thin film.

The Examiner's Action also relies on the teachings of Asada et al. The Action states that Asada et al. disclose a semiconductor device (67) having a peripheral driver circuit (driver IC 63) consisting of polycrystalline silicon thin-film transistors, a first interconnecting line formed as a thin film (conductor layer 71a along with the anisotropic conductive film 70a) extending from the semiconductor device to the driver IC, electrically connecting the input electrode (69) of the semiconductor device to the terminal (or output electrode 64) of the driver IC, and a second interconnecting line formed as a thin film (conductor layer 71b along with anisotropic [e.g., polysilicon] conductive films 70b and 70c) connecting the second terminal of the driver IC (input electrode 62 of driver IC 63) and the third terminal on the printed circuit board for supplying a power supply voltage and transmitting control signals (output electrode 74 of the printed circuit board 77) (FIG. 10B).

The Examiner's Action contends that Asada et al, as shown in FIG. 10B, disclose a thin IC disposed on a glass substrate 61. However, since an opposite substrate 66 is a substrate but not a thin film, the substrate 61 does not correspond to a substrate of claim 1 of the present application. Even if the opposite substrate 66 of Asada et al. were equated as being a first thin semiconductor film as recited in claim 1 of the present application, the driver IC 63

is not formed on the liquid crystal display substrate 65, which would then correspond to a substrate as recited in claim 1 of the present application, and is inseparably formed on the glass substrate 61a. Therefore, the opposite substrate 66 and driver IC 63 are not bonded to the same surface side of the same substrate. In other words, the driver IC 63 is not a second thin semiconductor film, as recited by claim 1, which is disposed on and bonded to the same surface side of the substrate.

In addition, the COG technique forms a transistor on a polysilicon layer formed by chip-on-glass technique inseparably with a glass substrate, and does not bond a polysilicon layer to the glass substrate. Therefore, a driver IC cannot be formed on a liquid crystal display substrate 65, and the liquid crystal display substrate 65 and the separate driver IC glass chip 61 must be electrically connected to each other.

Furthermore, the Examiner 's Action states that Asada et al. disclose a first interfacing line and a second interfacing line.

However, the conductive film 70a of Asada et al. connects electrodes 69 and 64, and does not connect a first thin semiconductor film and a second thin semiconductor film. Therefore, the first interfacing line, as recited in claim 1 of the present application, is not disclosed or suggested by Asada et al.

Further, and with respect to Applicant's dependent claim 6, the conductive layer 71b of Asada et al. connects a driver IC and another driver IC disposed on a separate substrate. In contrast, the second interconnecting line of claim 6

connects a circuit pattern formed on a substrate with a first thin semiconductor film and a second thin semiconductor film. Therefore, Asada et al. fail to disclose or suggest a second interconnecting line of claim 6 of the present application.

Therefore, Asada et al. fail to disclose or suggest the first and second interconnecting lines, as recited in claims 1 and 6 of the present application.

As described above, if the features disclosed by Norman et al. and Asada et al. were combined, the resulting configuration would not have a second thin semiconductor film, as recited in claim 1.

Therefore, even if the conductors 70a of Asada et al. were equated as being the first interfacing line of the present invention, the interfacing line would not include the features of claim 1 of the present application, namely, "extending from the first thin semiconductor film over said surface of the substrate to the second thin semiconductor film, electrically connecting the semiconductor device in the first thin semiconductor film to the first terminal in the second thin semiconductor film."

Since claim 1 includes features that are not disclosed or suggested by either Norman et al. and Asada et al., the invention of claim 1 is not obvious. It is thus requested that this claim, and the claims dependent therefrom, be allowed.

Further, dependent claims 2 and 3 are submitted to be patentably distinguishable over the cited references for at least the following additional reasons.

The Examiner's Action states that Norman et al. teaches a layer of conductive material (negative contact layer 13) disposed between the first thin semiconductor film (14) and the substrate (12), the layer of conductive material being bonded formed on the substrate and the first thin semiconductor film being bonded to the layer of conductive material, whereby the first thin semiconductor film is bonded on the substrate (Figure 1), and the layer of conductive material (13) being a metal layer (Column 2, lines 65-66).

In amended claim 2 of the present application, a layer of conductive material is disposed between the first thin semiconductor film and the substrate, the layer of conductive material is formed on the substrate, and the first thin semiconductor film is bonded to only the layer of conductive material, whereby the first thin semiconductor film is bonded to the substrate. Therefore, the first thin semiconductor film can be strongly and appropriately bonded to a flat surface of the layer of conductive material.

In contrast, and as shown in Figs. 2 and 4 of Norman et al., since the organic layer 15 is disposed on and across the stripe-shaped negative contact layer 13, the adhesive strength of the thin semiconductor film is weak. Therefore, the effect of the invention of claim 2 cannot be obtained by the device disclosed in Norman et al.

Regarding claim 10, the Examiner states that Norman et al. teaches that the first thin semiconductor film is an epitaxial grown compound semiconductor film (organic layer).

In Norman et al., the organic semiconductor is formed by a printing method such as an ink jet method or an evaporation method, but is not formed by an epitaxial growth method. In addition, there is no description in Norman et al. that a semiconductor device is formed by an epitaxial growth method

Regarding claim 14, the Examiner's Action states that Norman et al. teach the first thin semiconductor film includes only one semiconductor device (e.g., layer 15). However, as shown in Fig. 7 of Norman et al., the layer 15 is disposed across a plurality of negative contact layers 15, each intersection corresponds to a device, and a plurality of devices are formed within a single layer. Therefore, Norman et al. fail to disclose or suggest the first thin semiconductor film including only one semiconductor device.

Regarding claim 20, the Examiner's Action states that Norman et al. teach the first and second thin semiconductor films are less than or equal to ten micrometers thick (each of the layers 14 and 15 having a thickness of 200-700 angstroms or 0.02-0.07 micrometers).

A thickness of 200-700 angstroms indicates a thickness of an electron transport layer (that is, a kind of a wiring layer), but does not indicate a thickness of a thin semiconductor film. It is thus requested that these claims be allowed, and that these rejections be withdrawn.

The Examiner has also rejected claims 1, and 23-26 as being obvious in view of Koga et al. and Asada et al. It is submitted that these claims are patentable over the cited references for at least the following reasons.

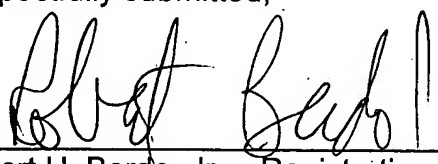
Koga et al. disclose an organic EL array exposure head and a printer. However, the light-emitting parts of the organic EL array exposure head are quite different from the combined semiconductor apparatus, as recited in claim 1. Thus, since this references does not overcome the above-noted deficiencies of the other cited references, even if the features recited by Norman et al. and Asada et al. were incorporated into the organic EL array exposure head of Koga et al., the combined semiconductor apparatus of claim 1 would not be obtained. It is thus requested that these claims be allowed, and that this rejection be withdrawn

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should the remittance be accidentally missing or insufficient, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



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